



Open Architecture Control Software

Watchdog Timer For SoftPLC

Application Note: SPZ-AN-1

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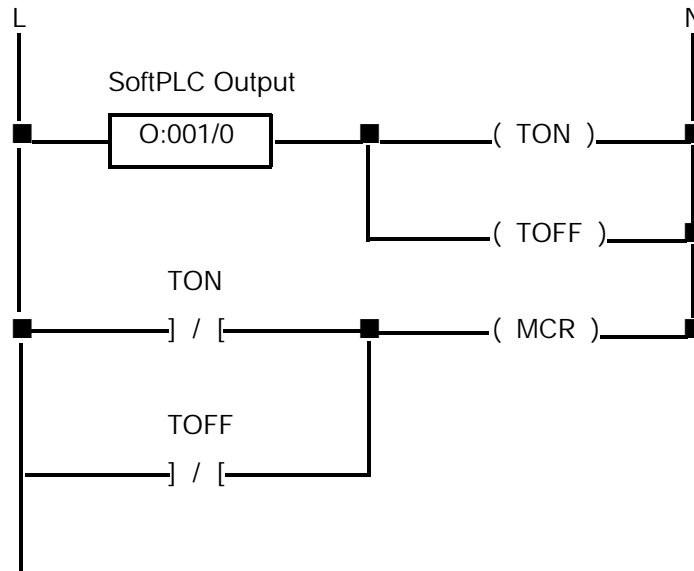
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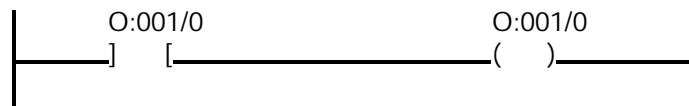
This application note describes how to wire an external watchdog timer circuit to SoftPLC. The purpose of the watchdog timer is to shut off power to Input/Output (I/O) Modules in case of scan loss due to software failure, hardware failure, abnormally long scan time and other causes. The ability to take such preventative action provides fault-tolerant operation of the SoftPLC system.

The circuit diagram below illustrates the actual wiring of the relays and the SoftPLC output:



In the above ladder logic representation of the watchdog timer circuit, there are two timed relays, TON and TOFF. TON starts timing on the positive going edge (FALSE to TRUE transition) of the output bit (in this example O:001/0 although any digital output can be used). Similarly, TOFF starts timing on the negative going edge (TRUE to FALSE transition) of the output bit.

Normally, there is a rung that toggles the state of O:001/0 in the SoftPLC ladder program as shown below:



O:001/0 toggles between FALSE and TRUE states from one scan to the next. As a result, TON and TOFF are restarted in each scan and MCR (Master Control Relay) that controls power to I/O Modules is kept energized since the parallel normally closed TON and TOFF relay contacts controlling the MCR always pass current.

However, when there is a scan loss because of a fault or hardware problem, SoftPLC does not execute the rung which toggles O:001/0. Timers TON and TOFF are not restarted and eventually expire at their preset periods. This cuts off current through the parallel TON and TOFF relay contacts; Master Control Relay is deactivated and power to I/O Modules is turned off.